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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,742	TRIVEDI ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/31/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-71 are presented for examination.

2. Claims 2,3,5,12,,13,,14,15,,30,,33,34, 46,49,50,61,62,65,66 are objected to because of the following informalities: the claim language "capable" is not a positive recitation of the claimed scope. Based on the broadest interpretation, "capable" could be "may". Applicant is suggested to use more defined language into the claims. Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1,2,9-13,219-22,24,25,27-29, 33,37-41,43-45,49,54,55,59-61,65,70,71 are rejected under 35 U.S.C. 102(b) as being anticipated by So (5,909,559).

4. As to claims 1, 19, 22, 24, 25, 27, 37, 40, 41, 53, 56, 57,69, So taught IC comprising at least :

a) a chip interconnect (see data path, see IC chip in Abstract) ;

b) a host interface [CPU port] coupled to the chip interconnect [data path] for interfacing the IC (see the VSP in fig.126) with the at least one host processor (see CPU in fig.126, or CPU in fig.127) external to the IC;

c) a memory interface [I/F port] coupled to the chip for interfacing the IC with the host memory [110] external to the IC;

d) a memory controller [DRAM controller 2250] coupled to the chip interconnect [data path] for controlling the host DRAM memory via the memory interface (see DRAM in main memory 110 in fig.57A,B, see col.8, lines 15-25, col.125, lines 54-56),

e) a scalar processing unit [VSP] coupled to the chip interconnect, the scalar processing unit being capable of executing instructions to perform scalar data processing (see VSP programmed to processing as scalar in col.26, lines 30-37);

f) a vector processing unit [VSP] coupled to the chip interconnect, the vector processing unit being capable of executing instructions to perform vector data processing (see VSP programmed to processing as vector in col.26, lines 30-37); ; and

g) input and output interfacing the IC with an I/O controller (not explicitly shown) of the data processing system, the I/O controller being external to the I/C for controlling I/O devices of the data processing system, wherein the chip interconnect [data path] , the memory controller [DRAM controller] , the scalar processing unit [VSP] , the vector processing unit [VSP], and the I/O interface (see the AGP and PCI ports) , the host interface [CPU port] and the memory interface [I/F port] implemented within the IC

which was a single chipset interfacing the at least one host processor host [CPU] and the host memory [main memory] (see fig.126).

5. So did not explicitly show the external I/O interface controller as clamed. However, So taught I/O busmaster form the host for performing the I/O transactions (see col.26, lines 10-16). Therefore, So must have external I/O controller.

6. As to claim 2,27,28,44,60 see the arbiter/data path in fig.127 for the switching mechanism for the data stream for vector and scalar processing .

7. As to claims 9,27,43, 59, see dispatched DSPops in col.26, lines 34-37.

8. As to claim 10, see VLIW in col.137, lines 1-5.

9. As to claim 11, So also disclosed a branch unit (see fig.21).

10. As to claims 12, 33,49,65, see fig.21 for the integer shifter and arithmetic unit.

11. As to claim 13, see floating point in col.32, lines 45-54.

12. As to claims 20, 38, 54, 70, see interrupt mechanism in fig.28A.

13. As to claims 21, 39, 55,71, see system memory map in col.23, lines 52-61.

14. As to claims 29, 45,61, see So fig.54 D,E for decoder.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 3,4 ,26,42,58 are rejected under 35 U.S.C. 103(a) as being unpatentable over So (5,909,559) in view of Morton (5,822,606).

16. As to claim 3, 4,26, 42,58, So did not specifically show the multiple scalar and vector processing units as claimed. However, Morton included processing instructions in multiple scalar units and multiple vector units simultaneously (see the parallel chips in col.13, lines 50-67). It would have been obvious to one of ordinary skill in the art to use Morton in So for including the multiple scalar and vector units simultaneously as claimed because the use of Morton could provide So the ability to accept multiple scalar and vector processing data a predetermined set of time slot, and therefore, expanding processing bandwidth of the system, and because So also taught a plurality of VSPs (see figs.122,123,126, see also col.155, lines 27-47) for multiple scalar and vector data processing (see also col.26, lines 30-37 for VSP used as scalar and vector processing), which was a suggestion of the need for providing multiple scalar and vector processing simultaneously in order to expanding the processing g bandwidth of the system, for doing so, provided a motivation.

17. Claims 5-8, 23, 30, 31 ,32,46-48, 62-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over So (5,909,559) in view of Beard (5,430,884) .

18. As to claims 5,23, 30,31,46,47, 62,63, So did not specifically showed his load and store unit (see fig.21 load/store) capable of executing instructions to load and store data from the general purpose registers as claimed. However Beard taught a load and store unit (LSU), the LSU being capable of executing instructions to load and store scalar data from and to the GPR, and the LSU being capable of executing instructions to load and store vector data from and to the VR (see f1g.17, load request and store request, see also col.30, lines 65-Q7). It would have been obvious to one of ordinary skill in the ad to use Beard in So for including the load and store unit as claimed because the use of Beard could provide So the capability to load and store data in the memory cache in response to a predetermined read/write command, such as load an or store, therefore, provided the access of the memory based on specific command defined by system, and because So also taught a load store unit though the detail of the load store not explicitly sown , one of ordinary skill in the art should be able to recognize the used of the load store unit for purpose of executing instructions to load and store scalar data from and to the GPR in order to accept specific type of read/write command.

19. As to claims 6, 31, 47, 63, Beard taught loads and stores data from and to the memory location (see memory location in fig.17.).

20. As to claims 7,32, 48, 64, See DMA in SO in col.120, lines 25-29.

21. As to claim 8, Beard also included bit length up to 32 (see col., lines 60-65).

22. Claim 14-18, 34 ,35,36, 50,51,52,66-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over So in view of Dowling (6,597,745).

23. As to clam 14,15,34,50, 66, So did not specifically sow the vector permute unit as claimed. However, Dowling taught system including a vector permutation (see col.13, lines 55-62) and complex integer (see complex integer in col.4, lines 1-8). It would have been obvious to one of ordinary skill in the art to use Dowling in So for including the vector permutation and complex integer as claimed because the use of Dowling could provide So the ability to accept more complex data calculation (e.g. vector permuting and integer addition with multiply etc.), thereby expanding the processing capability of So, and because So did disclose a multiplicity of add , shit and logical operation units (see fig.21), which was a suggestion of the need for including the a more complex arithmetic operations, such as vector permutation complex integer, for reducing the latency I the parallel processing. As to the vector floating point , see So's floating point in col.32, lines 45-54.

24. As to claims 16,35,51,67, see So's lookup table in fig.24A.

25. As to claims 17,36, 52, 68, See DMA in SO in col.120, lines 25-29.

26. As to claim 18, see So SARM in figs.50,51A.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a)Winegarden et al. (6,467,009) is cited for the teaching of the chipset interconnection (see fig.1) .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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